## REMARKS

### Status Of Application

Claims 1 and 11-22 are pending in the application; the status of the claims is as follows:

Claims 1 and 11-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,002,429 to Makioka et al. (hereinafter "Makioka") in view of U.S. Patent No. 5,978,020 to Watanabe et al. (hereinafter "Watanabe").

Claims 1 has been cancelled herein by this amendment.

### 35 U.S.C. § 103(a) Rejection

The rejection of claims 1 and 11-22 under 35 U.S.C. § 103(a), as being unpatentable over Makioka in view of Watanabe, is respectfully traversed based on the following.

### Claim 1

Claim 1 has been cancelled herein by this amendment. Thus, the rejection of claim 1 under 35 U.S.C. § 103(a), as being unpatentable over Makioka in view of Watanabe, is moot.

### Claim 11

Claim 11 recites a camera which can store in memory data of a taken image, comprising a detector for detecting whether or not said connection device is attached to said connector; and a controller for transitioning the camera into a state in order to output image data through said connector when said detector detects that said connection device is attached to said connector.

Makioka has been cited as teaching all of the present invention recited in claim 11 **except** a detector and controller for transitioning the camera into a state in order to output image data.

According to Makioka (with reference to Fig. 1), a digital camera operates to collect digital image data. The digital image data is stored in the frame memory of the camera. The digital image data is collected onto a memory card in synchronization with a system clock. Specifically, the subject of the digital image data is formed on a CCD 12 by an imaging lens 11, and the CCD 12 outputs an analog video signal which represents the image of the subject. The analog video signal is applied to a preprocessing circuit 13. The output from the preprocessing circuit 13 is applied to an analog/digital (A/D) converting circuit 14, where the signal is converted into a digital image data. (Makioka, column 4, lines 26-34.) **Y/C Signal = Image Data (Data Format Conversion)**. The digital image data converted by the A/D converting circuit 14 is stored temporarily in the frame memory 16. The luminance-data/chrominance-data (Y/C) processing circuit 18 separates the digital image data into luminance data and chrominance data. Then the digital image data in the form of the luminance data and chrominance data are stored in the frame memory 16 again. (Makioka, column 4, lines 35-47.) The digital image data stored in the frame memory is then compressed to be stored into the memory card. When the data is reproduced, the digital image data is read out of the memory card 1 and decompressed by circuit 17. The decompressed image data is stored in the frame memory 16 again under the control of the memory controller 40. (Makioka, column 4, line 60- column 5, line 3.) When the digital image data has been recorded on the memory card for reproduction, the system clock generating circuit 20 outputs a clock signal having a certain frequency, and each circuit block operates in synchronization with the clock signal. Under the control of the memory controller 40, the digital image is read from the frame memory 16 while the pixel data is thinned out (embodiment 1) or averaged (embodiment 2) for display. According to Makioka, the array of pixel data is thinned or averaged to a number less than the number of pixel data input prior to being displayed. This thinning is done because the number of pixels in the playback mode is less than the number of pixels in the photographic mode, and the frequency of the clock signal applied to each circuit block is

less than in the photographic mode. (Makioka, column 5, lines 9-15.) In the playback mode, each circuit is operated by a clock signal having a frequency which is half of the clock signal in the photographic mode. This makes it possible to keep the amount of power consumed low in the playback mode. (Makioka, column 6, line 65- column 7, line 2.) The image data is then subjected to processing through Y/C circuit 18. The playback circuit 19 converts the digital image data inputted thereto into an analog signal for display on the monitor display unit 2. (Makioka, column 5, lines 16-23.) In the playback mode, the digital image data is read out of the frame memory 16 and applied to the playback circuit 19 through the Y/C processing circuit 18. In the playback circuit 19, the thinned digital image data input thereto is converted into an analog video signal and then amplified for display on monitor display unit 2. (Makioka, Column 5, lines 4-3.) Thus, not only does Makioka not disclose or suggest any detector and controller for transitioning the camera into a state in order to output image data, Makioka also doesn't disclose or suggest a camera which stores data of a taken image in memory.

In an attempt to overcome the inadequacies of Makioka, Watanabe is cited in combination therewith. Watanabe is cited as teaching using an image pickup system that comprises a CPU working in combination with an interface and detects a connection between monitor 7 and the camera so as to process image data in accordance with characteristics of monitor 7 (Watanabe, column 10, lines 62-67 and column 11, lines 25-55.) Further, Watanabe is cited as teaching a control unit 17 controls DSP 13 that processes image data so as to output image data matched to the display 7 (column 11, lines 47-63.)

Watanabe does not disclose or suggest that the camera store the **taken image** in a memory. As will be discussed in greater detail below, the camera of Watanabe merely temporarily stores the **reduced image data**. As described in Watanabe, an image pickup system is composed of at least one image pickup unit, at least one computer, and a pick-up image signal processing apparatus. (Watanabe, column 2, lines 22-31) The image pickup system of Watanabe is configured in any one of thirty-four (34) different options (display methods) as disclosed in column 2, line 34- column 5, line 49. In one embodiment of

Watanabe, the image pickup system is disclosed to provide a varying control means for varying an image pick-up action of the image pick-up device based on a comparison of the processor speed of the computer and the image pick-up speed of the image pickup unit. (Watanabe, column 2, lines 34-52) Watanabe only generally (i.e., non-specifically) discloses the various methods or actions which can be varied. These include: varying the selected pixels for displaying (5); varying the number of frames of images to be picked up per unit time (i.e., the image pickup rate) (6); selecting only one picture for display from among a plurality of pictures (7); selecting fewer than all of the plurality of pixel rows for display (8); decreasing the number of colors per frame (9); and decreasing the amount of information carried by each pixel (10). According to embodiment (20), the image pick-up unit of the image pickup system includes display speed detection means for detecting or predicting a display speed of an image display device included in the connected external apparatus (the computer); and according to (26) the control means is arranged to receive information on a display capability of a display device included in the external signal processing apparatus (i.e., the computer). That is, according to the various embodiments of the image pickup system disclosed in Watanabe, the image pickup system is generally stated to vary the quantity and/or quality of image data picked up by the image pickup unit transferred for display on the computer based upon a variety of determination methods or schemes. Watanabe states that the purpose of this is to match the capabilities of the display device (e.g., computer) and the capability of the image pick-up device **so that only the matched number of pixel data is picked-up, processed, and transferred to the display device**. By picking up or processing no more data than the computational device is capable of processing or the display device is capable of displaying, the size of the image processing unit can be decreased and the size of the image pickup unit can be reduced so that it can be formed as a card and adapted to be received in a conventional computer slot. According to Watanabe, the camera unit 1 receives an image and adjusts the number of pixels or quality of the pixel data (e.g., only monochrome tones instead of color) by one of the methods disclosed above. The reduced number of pixels or quality of data is stored (temporarily) in the FIFO memory 14 (which simply acts as a buffer). (Watanabe, column 11, lines 39-56.) The images are simply transferred from the FIFO

memory 14 to the display 7 via the computer 3. Thus, the stored image data of Watanabe is **not** the **taken image** in the first format, but a reduced quantity of the taken image data.

Additionally, Watanabe discloses matching the DSP processing to the number of pixels of the display method of the display device, since Watanabe assumes that the number of pixels of the picked-up image data is larger than the number of pixels that can be displayed by the display device 7. Watanabe does not disclose or suggest that this operational characteristic information is obtained. (Watanabe, column 11, lines 39-42.) Watanabe only discloses accomplishing this by dividing the number of pixels of the picked-up image data outputted from the image pick-up unit by two prior to submission to the display device. (Watanabe, column 11, lines 42-46.) The **actual** display characteristics of the display device are not considered in this calculation. Thus, the same image data cannot be simultaneously displayed on two different display devices having different resolution characteristics.

Further, Watanabe discloses sending information on the **display method** of the display device to the control unit. The DSP 13 performs a processing to match the number of pixels of the pickup image data to the amount of information that can be displayed by the display device 7. This is accomplished by reducing the number of pixels of image data to be displayed by one of the 34 various image pickup system display methods disclosed in Watanabe. However, this is not the same thing as a detector and controller for transitioning the camera into a state in order to output image data through said connector when said detector detects that said connection device is attached to said connector. Watanabe **does not** disclose or suggest a controller for **transitioning the camera into a state** in order to output the image data. Watanabe merely discloses reducing the quantity and quality of the data to be transferred for display.

Neither Makioka nor Watanabe disclose the same element of claim 11, that being a controller for **transitioning the camera into a state** in order to output the image data. Thus, claim 11 is not rendered obvious by a combination of Makioka and Watanabe. As

claims 12-15 depend therefrom, they too are not rendered obvious by Makioka or Watanabe, either singly or in combination.

**Claim 16**

Claim 16 recites a detector for detecting whether or not said connection is attached to said connector, whereby, when said detector detects that said connection device is attached to said connector, the camera system is transitioned into a state in order to output stored image data to the external apparatus.

Thus, for at least the reasons presented above with respect to claim 11, claim 16 is not rendered obvious by Makioka or Watanabe, either singly or in combination. As claims 17-22 depend therefrom, they too are not rendered obvious by Makioka or Watanabe, either singly or in combination.

Accordingly, it is respectfully requested that the rejection of claims 11-22 under 35 U.S.C. § 103(a) as being unpatentable over Makioka in view of Watanabe, be reconsidered and withdrawn.

## CONCLUSION

Wherefore, in view of the foregoing amendments and remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

This Amendment does not increase the number of independent claims, does not increase the total number of claims, and does not present any multiple dependency claims. Accordingly, no fee based on the number or type of claims is currently due. However, if a fee, other than the issue fee, is due, please charge this fee to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260.

Any fee required by this document other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be construed as also constituting a Petition for Extension of Time Under 37 C.F.R. § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any other fee required for such Petition for Extension of Time and any other fee required by this document pursuant to 37 C.F.R. §§ 1.16 and 1.17, other than the issue fee, and not submitted herewith should be charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

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July 11, 2003

DA1 263276v5